

REMARKS

Allowable Subject Matter

The Examiner states:

Claims 10-12, 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: cited references do not teach or mention applicant's claimed limitation, "divider for dividing by 3 and providing a divisor and remainder" in claim 10 and 19.

Applicant acknowledges that the Examiner has indicated allowance of claims 10-12 and 19-20 if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant notes that other claims are also patentable for the reasons set forth below.

35 U.S.C. § 102

The Examiner rejected claims 1, 4-9 and 13-16 under 35 U.S.C. 102(b) as being anticipated by Koyama et al. (US Patent 6,597,349).

Claim 1

The Examiner states:

**As to claim 1, Koyama discloses an active matrix display, comprising:
an array of pixels provided over a common substrate (see Fig. 10A), each pixel comprising a display element and a switching device (Fig. 10(1002); and
a column driver (Fig. 10(1003)) for providing signals to the pixels for driving the display elements, the column driver comprising digital to analogue converter circuitry (see Fig. 2(208)) and providing a first number of display element drive levels greater than 2,
wherein each pixel comprises means for converting the first number of display element drive levels (Fig. 15(1507)).**

Applicant notes that Koyama does not describe and would not have made obvious "each pixel comprises means for converting the first number of display element drive levels into a second, greater number, of pixel grey levels," as recited in claim 1.

The Examiner points to FIG. 15 element 1507 as disclosing the limitation in claim 1 recited above. However, element 1507 is a level shifter circuit that raises the voltage level of the digital video data (col. 21, lines 25-26), and does not convert a first number of display element drive levels into a second, greater number, of pixel grey levels.

Koyama describes a driving circuit of a display in which source signal lines are driven in a time-division manner to decrease the number of D/A conversion circuits and reduce the size of the semiconductor display device (Abstract). Koyama describes reducing the number of D/A converters, but does not convert a first number of drive levels to a second, greater number, of pixel grey levels.

Koyama describes a semiconductor display device having a memory circuit for storing m x-bit digital gradation signals (m and x are natural numbers), and n D/A conversion circuits (n is a natural number) for making analog conversion of the m x-bit digital gradation signals supplied from the memory circuit and for supplying analog signals to m source signal lines. Each of the n D/A conversion circuits sequentially makes analog conversion of the m/n x-bit digital gradation signals to supply converted signals to corresponding m/n source signal lines. See column 3, lines 4-14. In Koyama, the digital gradation signals remain x-bit and do not change. Therefore, Koyama does not disclose or suggest converting a first number of drive levels to a second, greater number, of pixel grey levels.

35 U.S.C. 103

The Examiner rejected claims 2-3, 17-18 and 21-25 as being unpatentable over Koyama in view of Silverbrook et al. (U.S. Patent 5,805,136).

Claim 17

The Examiner states:

As to claim 17, Koyama discloses a method of driving an active matrix display, comprising:

providing first and second drive voltages to a display pixel having first and second display elements (Fig. 2(S0, S1)), the first and second drive voltages being selected from two adjacent drive voltage levels of a digital to analogue converter (Fig. 2(208)) which has more than 2 output levels (Fig. 2(210)).

However Koyama does not teach within the pixel, generating an intermediate grey level corresponding to a drive voltage between the first and second levels.

Silverbrook discloses an intermingling sub-pixels in discrete level display wherein teaches intermediate grey level (See Fig. 17, 16 different levels).

It would have been obvious to one ordinary skill in the art at the time of invention was made to incorporate generating intermediate grey level as in Silverbrook into semiconductor display device of Koyama, because a pixel layout design for a discrete level display providing a interfused arrangement of more intense member (see Col. 2 lines 6-19).

Koyama does not describe and would not have made obvious “providing first and second drive voltages to a display pixel having first and second display elements, the first and second drive voltages being selected from two adjacent drive voltage levels of a digital to analogue converter,” as recited in claim 17.

First, the Examiner appears to contend that display elements S0 and S1 in FIG. 2 of Koyama correspond to the first and second display elements of a display pixel in claim 17. Applicant disagrees. In Koyama, the source signal lines are given reference characters of S0 to S1919 (col. 5, lines 22-25). Koyama describes an example display having a display resolution of 1920 x 1080 (col. 4, lines 54-56), and FIG. 2 shows source signal lines S0 to S1919, so the reference characters S0 and S1 refer to two source signal lines that control the gray level of two pixels, not two display elements of a display pixel.

Second, Koyama does not disclose or suggest that the drive voltage levels on the source signal lines S0 and S1 are selected from two adjacent drive voltage levels of a digital to analogue converter. Koyama does not disclose or suggest that the voltage levels on signal lines S0 and S1 have any relationship with each another. Since each pixel can have any gray level, it can be inferred that the drive voltage levels on the source signal lines S0 and S1 can be any two different levels, and are not necessarily selected from two adjacent drive voltage levels of a digital to analogue converter.

The Examiner acknowledges that Koyama does not disclose “within the pixel, generating an intermediate grey level corresponding to a drive voltage between the first and second levels,” but points to Silverbrook as disclosing what is missing in Koyama. Applicant disagrees.

Silverbrook discloses a pixel arrangement in FIGS. 16 and 17 in which each pixel is driven by 4 drive lines that independently drive 4 illumination areas to generate 16 gray levels. However, Silverbrook does not disclose or suggest that any of the illumination levels generated by the pixel of FIGS. 16 and 17 is an “intermediate grey level” corresponding to a drive voltage between the first and second levels selected from two adjacent drive voltage levels of a digital to analogue converter. Rather, it is likely that each illumination level generated by the Silverbrook pixel corresponds to one of the drive voltage levels of a D/A converter.

Therefore, Koyama and Silverbrook do not describe or suggest “within the pixel, generating an intermediate grey level corresponding to a drive voltage between the first and second levels, in which the first and second drive voltages are selected from two adjacent drive voltage levels of a digital to analogue converter,” as recited in claim 17.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner’s position with respect to that claim or other claims.

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Please apply \$130 for the Petition for Extension of Time fee, and any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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